PT68K5

User's Manual

Peripheral Technology
1250 E. Piedmont Rd.
Marietta, GA 30062

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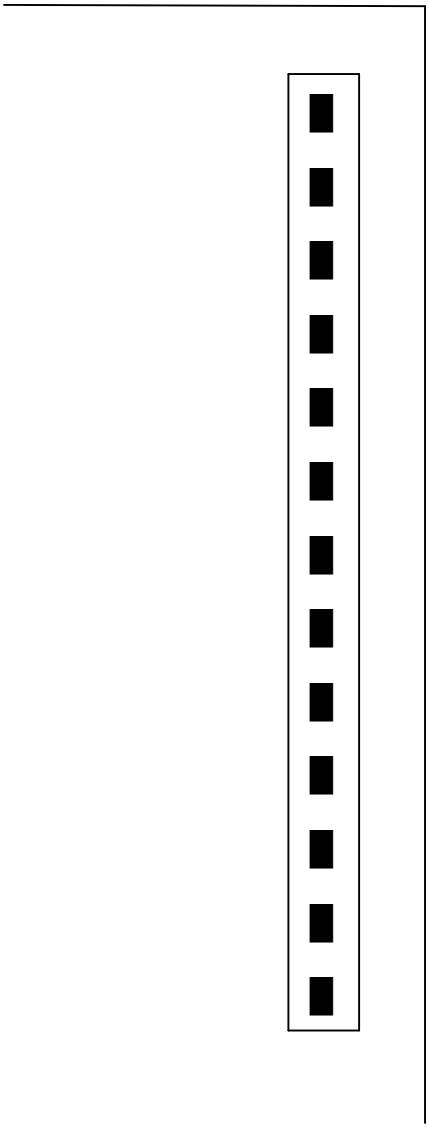
POWER CONNECTION

Connect power to the system board. The power connector is J12.



Monitor Choice

Either a VGA monitor with IBM keyboard and/or RS232 terminals may be used with the CD68X20 computer. Currently an ET4000 VGA adaptor card should be used. Boards containing the OAK 037 chip will work in text modes only. If graphics is a consideration the ET4000 VGA card should be used. Currently OS9 drivers and ROM code will support CGA and some EGA cards. CGA and EGA cards may not be supported in the future. If an RS232 terminal is the only monitor type it should be connected to COM1 (J19). If no RS232 terminal is used a modem should not be connected to COM1. Use COM2, COM3 or COM4 for modems.

RS-232 TERMINAL INSTALLATION

Connect a cable between COM1 (J19) and the CRT. See Page 4, "RS-232 Interface" for more information on cabling. The COM1 port is the MAIN terminal port. The use of COM2, COM3 or COM4 is determined by the operating system.

IMPORTANT: Some of the monitors/operating systems may allow operation with a three wire cable; most will require a four wire cable (CTS). A common complaint is the system works with REX but not with OS9. This is because OS9 requires a four wire connection to operate properly. The OS9 boot menu will be displayed with a three wire cable, but OS9 itself requires a four wire cable.

VGA MONITOR INSTALLATION

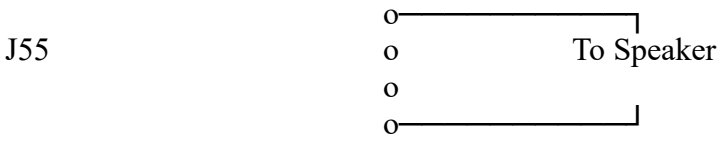
1. Install an IBM compatible adaptor card in one of the IBM compatible I/O slots.

2. Plug a VGA monitor into the display adaptor card.

3. Plug an IBM PC/XT compatible keyboard into keyboard connector J10. The keyboard must be set to **XT mode** if it has an XT/AT switch position.

Speaker Connection

Plug the speaker into J55.



IDE Interface

The CD68X20 has a built-in 16-bit IDE interface. IDE drives are connected with a 40 conductor ribbon cable to J47. Pin 1 is marked by a dot on the motherboard. IDE drive activity may be shown by connecting an LED to J54. Most IDE drives have a jumper that enables the LED activity line. Check your drive installation manual if the LED (J54) does not work. For more specific information on the IDE interface check the installation instructions supplied with the operation system(s) that you are installing.

SCSI Interface

SCSI drives are connected to the CD68X20 by a 50 conductor cable to J11. Pin 1 is marked by a dot on the motherboard. Additional information on use of SCSI drives will be included with the operating system(s) you are installing.

LED CONNECTION

Most XT/AT cabinets have a panel with POWER, TURBO and HARD DISK LEDS. We suggest using the Turbo LED as the HALT light indicator. The appropriate wires should be plugged into the appropriate pins on your CD68X20 system board.

J53 - Power
J48 - Halt Status
J47 - IDE Drive Activity

Connect the power LED to J53.

Connect the Turbo mode LED to J48 (HALT STATUS). NOTE: the HALT LED will light for a second when turning the computer on or when pressing the reset switch.

The LED plugs are usually not polarized, so it will be necessary to reverse the connector if the LED's don't light. The LED's will not be damaged if the plug is installed incorrectly.

RESET SWITCH CONNECTION

Plug the connector from the reset switch to J2 (CDS68020 module) on the Processor module.

SYSTEM STARTUP

The sign-on message and procedures for starting the CD68X20 computer will vary depending on the operating system(s) that have been selected. A supplemental sheet or manual should be provided for each operating system detailing the start-up procedure for the CD68X20.

Floppy Interface

The floppy interface can support up to two floppy drives. It will support 360K, 720K, 1.2M, 1.4M and and 2.8M floppies in either 3.5" or 5.25" sizes. NOTE: Support of 2.8M sizes requires special disk drivers and the plus version of the 37C65 chip. The floppy interface requires the use of an IBM AT-type floppy cable. The IBM-type cable is easily identified since part of the wires are twisted between the two floppy connectors. All drives used with the CD68X20 should be configured as the second drive. (Drive 1 if the drive numbering starts with 0). Most drives are already configured for an AT compatible and should work properly on the CD68X20 with no jumper changes. The floppy cable determines which drive is 0 and 1. The drive on the end of the cable (the one that gets the twisted cable) is drive 0. The connector in the middle is Drive 1.

RS-232 INTERFACE INFORMATION

Connectors J16, J17, J18, J19

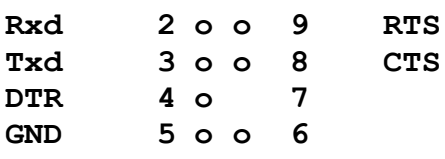
PIN	DESCRIPTION
1	Data Carrier Detect (DCD)
2	Received Data
3	Transmitted Data
4	Data Terminal Ready (DTR)
5	Ground
6	No Connection
7	Key
8	Clear To Send (CTS)
9	Request to Send (RTS)
10	No Connection

TYPICAL CRT TO COMPUTER CONNECTION

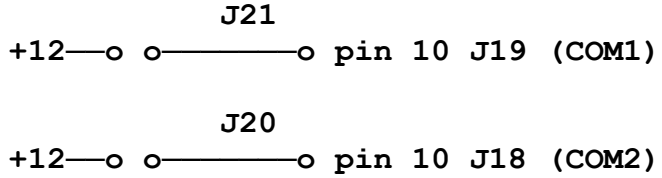
Pin	J16, J17, J18 or J19	DB25 Pin
2	o——————o	2
3	o——————o	3
5	o——————o	7
8	o——————o	20

Note: CTS must be connected for the RS-232 interface to work. CTS should be connected to +12V if no signal is available from the terminal.

(COM connectors viewed from component side)



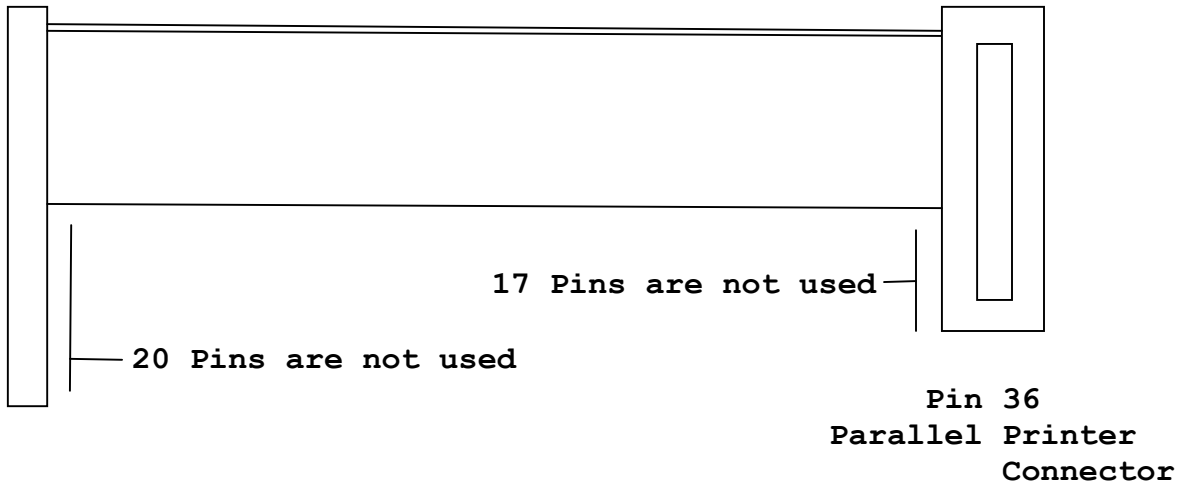
NOTE: +12V can be fed to Pin 10 of J18 and J19 by installing a shunt on J20 or J21.



PRINTER INSTALLATION

Printers are usually connected to the CD68X20 by using the MC68230 PIA (J42). Some operating systems may support printers connected to a printer port on an IBM type card. The preferred method to connect a printer is to use the Printer Port (J42).

The PIA port (J42) is arranged to allow IDC connectors to connect between J42 and the printer connector. To construct a cable use 20 conductor cable and follow the diagram below.



40 Pin female IDC connector

NOTE: This cable would usually have a DB25F and DB25M connector installed between the 40 pin IDC connector and the 37 pin parallel printer plug.

Memory Installation

The CD68X20 has a 32 bit wide memory bus requiring a minimum of 4 SIMMS but may contain up to 8 SIMMS. In all cases the CD68X20 requires either 4 or 8 SIMMS to function. PAL U29 determines the size of the SIMM that can be used. The standard PAL Supports 1MB and 4MB SIMMS. All SIMMs should have an access time of 60ns or less.

Bank 1	Bank 2
SIM0	SIM1
SIM2	SIM3
SIM4	SIM5
SIM6	SIM7

SIMM size	1 Bank	2 Banks
256K	1M	2M
1M	4M	8M
4M	16M	32M
16M	64M	128M

J51 Open = 1MB SIMMS Shorted = 4MB SIMMS

XT/AT Card IRQ's

Motorola 68xxx microprocessors use an active low, level sensitive IRQ structure. XT/AT cards, however, use an active high IRQ. Also some customers have produced custom cards for the XT slots that use the Motorola interrupt structure. The CD68X20 can be configured to use either active high or active low IRQ's for the XT/AT cards. However once the low or high level is selected, this level will be used on all cards for that interrupt level. IRQ levels are not individually selectable for each card. The jumper list to select various IRQ's is shown below.

Processor IRQ	XT Non-Inverted	XT Inverted
IRQ 3	J22	J24
IRQ 4	J26	J25
IRQ 5	J31	J32
IRQ 6	J35	J34
IRQ 7	J28	J29

Note: If the non-inverted XT IRQ is selected the inverted may not be selected and vice versa.

Processor IRQ	AT CARD IRQ	AT Inverted
3	10	J24
4	11	J27
5	12	J33
6	14	J34
7	15	J30

Installing jumpers connects the XT/AT IRQ's to the processor IRQ's. Unless you have a driver that requires one of these IRQ's none of the IRQ enable jumpers should be installed.

Jumper/Configuration Options

J1-J7	-	IBM XT Slots
J8	-	High Density Floppy Connector
J9	-	ALT86 Interface
J10	-	PC/XT Interface Connector
J11	-	SCSI Connector
J12	-	Power Connector
J13	-	IRQ from SCSI chip (jumper to enable) NOT TESTED AT THIS TIME
J14	-	Floppy Drive Disable (Shorted=Disabled)
J15	-	Clock for WD37C65 (16MHZ or 32MHZ)
J16	-	COM 4 Port
J17	-	COM 3 Port
J18	-	COM 2 Port
J19	-	COM 1 Port
J20	-	Enable +12V on Pin 10 J18 (COM2)
J21	-	Enable +12V on Pin 10 J19 (COM1)
J22	-	Shorted = NIRQ3 from XT connector (J1-J7) to processor NIRQ3
J23	-	Shorted = Inverted IRQ10 from AT connector to processor NIRQ3
J24	-	Shorted = Inverted IRQ3 from XT connector to processor NIRQ3
J25	-	Shorted = Inverted IRQ4 from XT connector to processor NIRQ4
J26	-	Shorted = IRQ4 from XT connector to processor NIRQ4
J27	-	Shorted = Inverted IRQ11 from AT connector to processor NIRQ4
J28	-	Shorted = IRQ7 from XT connector to processor NIRQ7
J29	-	Shorted = Inverted IRQ7 from XT connector to processor NIRQ7
J30	-	Shorted = Inverted IRQ15 from AT connector to processor NIRQ7
J31	-	Shorted = IRQ5 from XT connector to processor NIRQ5
J32	-	Shorted = Inverted IRQ5 from XT connector to processor NIRQ5
J33	-	Shorted = Inverted IRQ12 from AT connector to processor NIRQ5
J34	-	Shorted = Inverted IRQ6 from XT connector to processor NIRQ6
J35	-	Shorted = IRQ6 from XT connector to processor NIRQ6
J36	-	Shorted = Inverted IRQ14 from AT connector to processor NIRQ6
J37-J41		IBM AT Slots
J42	-	Printer Port (MC68230)
J43	-	J43-J44 U34 SRAM Size
J44		"
J45	-	Processor Card
J46	-	A26 to SIMM's (If jumpered connect A26 to SIMMS. J51 must not be installed if this jumper is used.)
J47	-	IDE Connector
J48	-	HALT LED
J49	-	DRAM memory DTACK size (Should be shorted)
J50	-	DRAM memory DTACK size (Should be shorted)
J51	-	Shorted = 1MB SIMMS; Open = 4MB SIMMS
J52	-	This jumper cancelled due to engineering changes
J53	-	Power LED
J54	-	IDE LED
J55	-	Speaker
J56	-	Clock to SCSI chip (position 1=16MHZ, position 2=opt clock U4)

CDS68020 Memory Map

```
68020 Processor, 25MHZ Clock, DRAM should be 60ns

00000000-001fffff   DRAM 256Kx9 SIMM    (2MB Total)
          or
00000000-007fffff   DRAM 1Mx9 SIMM      (8MB Total)
          or
00000000-01ffffff   DRAM 4Mx9 SIMM      (32MB Total)
          or
00000000-07ffffff   DRAM 16Mx9 SIMM     (128MB Total)

08000000-0fffffff   IBM Slot Memory
10000000-17ffffff   IBM Slot I/O Ports
18000000-1fffffff   EPROM Space
20000000-27ffffff   68XXX Peripheral Space

100003f2       WD37C65

20000000-200007ff   MK48T02 Clock/2K Battery Backed-up RAM
20004000-2000403f   MC68681 DUART (COM1 and COM2)
20004040-2000407f   MC68681 DUART (COM3 and COM4)
20004080-200040bf   MC68230
200040C0-200040ff   WD33C93 SCSI Chip
20004100            IBM Keyboard Data Register
20004101            Clear IBM Keyboard Data Available
20004140-2000417f   DAC Chip
20004180-200041bf   IDE Controller Chip Select 1
200041c0-200041ff   IDE Controller Chip Select 2
20008000-2000ffff   32Kx8 Static RAM
```

NOTE: The first 8 locations of EPROM (18000000-18000007) are mapped to address 0 after a reset. After eight "AS" strobes, DRAM is restored to the first eight locations.

The XT/AT slots appear as contiguous memory to the 68xxx processor.

Memory Use of MK48T02

```
20000000-200007df   RAM Currently Available For Use
200007e0-200007f7   Reserved For Use by Computer Design
200007f8-200007ff   Clock Registers

200007e1            Boot Device
200007e2-200007e3   Baud Rate
200007e4            Floppy Type
200007e5            Debug Flag (0=don't use debugger, ff=use debugger)
200007f0            Floppy Motor on Timer (OS9)
```

MK48T02 Timekeeper Clock
Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0	Function	
200007ff	-	-	-	-	-	-	-	-	Year	00-99
200007fe	0	0	0	-	-	-	-	-	Month	01-12
200007fd	0	0	-	-	-	-	-	-	Month	01-12
200007fc	0	0	0	0	0	-	-	-	Day	01-07
200007fb	0	0	-	-	-	-	-	-	Hour	00-23
200007fa	0	-	-	-	-	-	-	-	Minutes	00-59
200007f9	ST	-	-	-	-	-	-	-	Seconds	00-59
200007f8	W	R	S	-	-	-	-	-	Control	

ST = Stop Bit
W = Write Bit
R = Read Bit
S = Sign Bit

Reading the TIMEKEEPER

When reading the clock registers, no updating of the register is desired until after the time/date data can be read. Halting the updating of the TIMEKEEPER registers is performed by writing a 1 into the "Read" bit. As long as a 1 remains in that position, updating is halted. It is resumed as soon as the bit is reset to a "0".

Setting the TIMEKEEPER

Each of the TIMEKEEPER registers are actual read/write static RAM memory locations. They can be written at any time. Of course, in normal operation, the date written there is over-written every second by the TIMEKEEPER. So accidental writes to the TIMEKEEPER registers will not corrupt the clock. Nevertheless, when it comes time to set the clock, that is exactly how it is done; and another bit in the Control byte allows it to happen. The eighth bit of the Control register is referred to as the "Write" bit. Setting the Write bit to a "1" halts updates to the TIMEKEEPER registers. The user can then load the registers with the correct day, date, and time data. Resetting the Write bit to a "0" transfers those values to the TIMEKEEPER counters and allows normal operation to resume.

Calibrating the TIMEKEEPER

The TIMEKEEPER will typically, without calibration, run within about 1.53 minutes per month. The TIMEKEEPER may be calibrated by changing the calibration byte. The calibration byte occupies the five lower order bits in the Control register. The byte can represent any value between 0 and 31 in binary form. The sixth bit is a sign bit. Each of the calibration bits in the calibration byte represents 5.35 seconds per month. Increasing the count value speeds the clock up; subtracting from it slows it down.

I/O Slot Addressing

The Motorola 68020 and 68030 microprocessors have dynamic bus size selection. This allows cards with either a 8 or 16 bit bus to appear as a continous addressed device. The switching is done automatically and is totally transparent to the user and user programs.

Memory addresses and I/O port addresses listed in AT peripheral card documentation can easily be converted to addresses as used by the CD68X20.

For memory addresses: $08000000 + address of peripheral card.

For I/O addresses: $10000000 + I/O address of peripheral card.

For example if an I/O register is listed as having a port address of 3D4 the address as seen by the CD68X20 is $100003D4.

Software Considerations

The CDS68020 runs at 25MHZ with 0 wait states and has a processor cache that allows some instructions to appear to execute in 0 clock cycles. This high speed may cause problems when accessing peripheral chips. When loops with a test and branch instruction are executed the 68020 is able to access the peripheral chip on consecutive bus cycles. Many peripheral chips do not work properly when accessed this fast. When most of the chips were designed it was assumed that once a register was read there would be several processor cycles before the register could be read again. Chip data sheets may or may not give the minimum time before reading a register twice in a row. The safest way to deal with this program is to put in delay when writing new software drivers. The delay can later be removed and the driver retested if more speed is desired.

The code below may not work properly on many devices.

```
loop  tst.b #ReadyBit,StatReg(a3)
      bne.s loop
```

The code below is one way the above code could be modified to work with the CDS68020.

```
loop  tst.b #ReadyBit,StatReg(a3)
      nop
      nop
      nop
      bne.s loop
```

Other changes may include turning the instruction cache off for the 68020 and 68030 processors when executing driver code. When executing driver code on the 68030 the data cache must be turned off.

DAC Interface

The CD68X20 has an 8 bit DAC chip. The DAC chip feeds an audio amplifier chip with a power of 700mw. The DAC chip does not require any initialization. Values between 0 and 255 are written to address $20004140. The DAC can be used to synthesize tones or to play digitized audio.

CD68X20 System Board Parts List

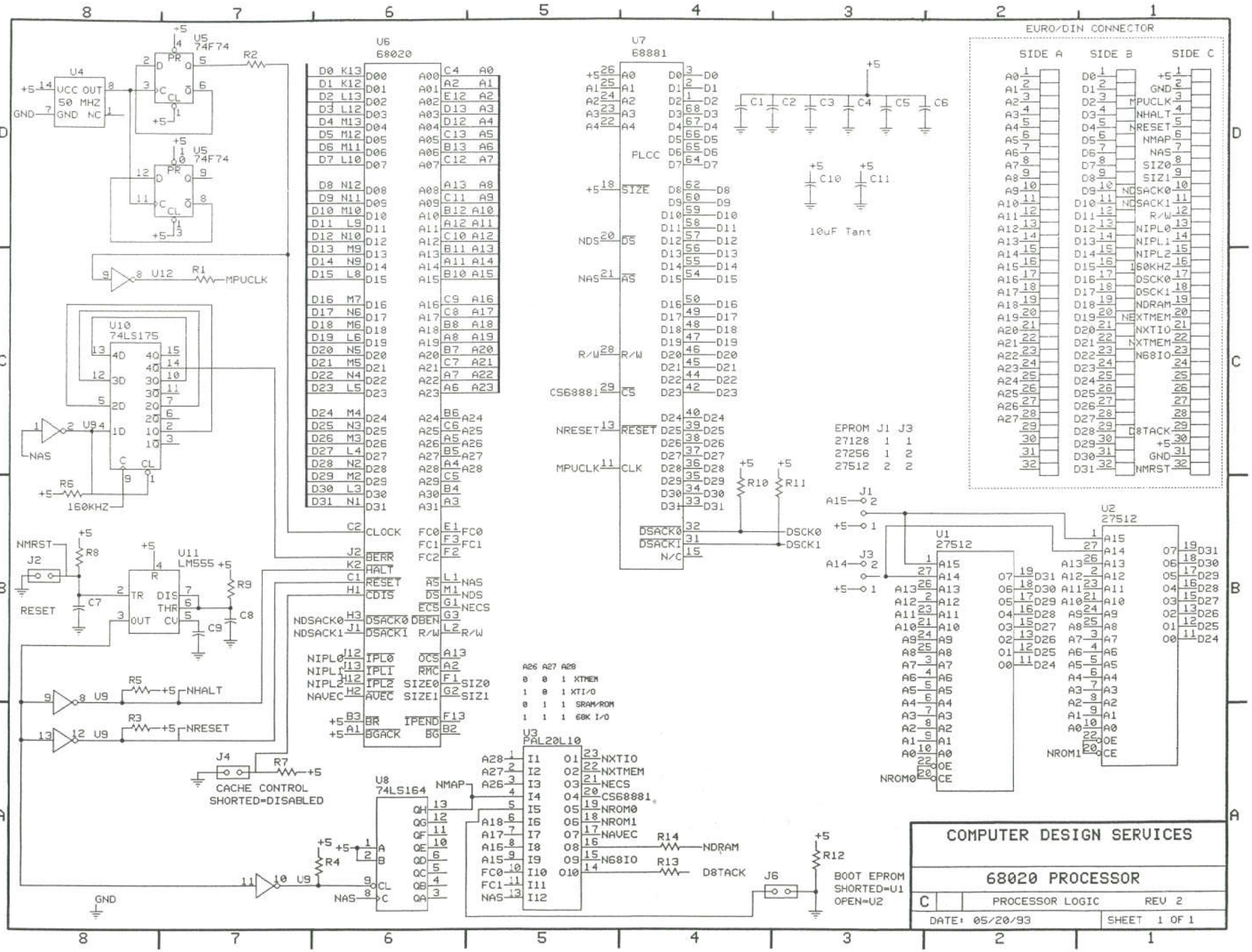
1	U1	14.318MHZ OSC
1	U2	3.6868MHZ OSC
1	U3	9.6HZ OSC
1	U4	40MHZ OSC
1	U5	SMC37C65C+P
4	U6,U8,U42,U50	74F74
1	U7	WD33C93B-PL (Optional)
1	U9,U37	TIBPAL16L8-15CN
1	U10	32MHZ OSC
3	U11,U13,U57	MC1489
3	U12,U14,U58	MC1488
3	U15,U16,U41	7406
1	U17	MC68230P8
2	U18,U19	MC68681P
1	U20	74LS148
4	U21,U22,U23,U28	74F373
4	U24,U25,U44,U45	74LS245
2	U27,U29	TIBPAL22V10-15
1	U30	74LS367
1	U31	MX7524JN
1	U32	74LS322
1	U33	MK48T02
1	U34	32Kx8 SRAM (Optional)
3	U35,U36,U43	74F257
1	U38	74F04
1	U39	74LS30
1	U40	74LS138
1	U46	74F175
1	U47	74F32
1	U48	74S10
1	U49	74F11
1	U51	74LS175
1	U52	LM386N
1	U53	75ns Delay Line
1	U54	74LS390
1	U55	74F00
1	U56	74F02
1		60NS Delay Line
7	J1-J7	62 Pin XT Connector
1	J8	17x2 Header Strip
5	J9,J16-J19	5x2 Header Strip

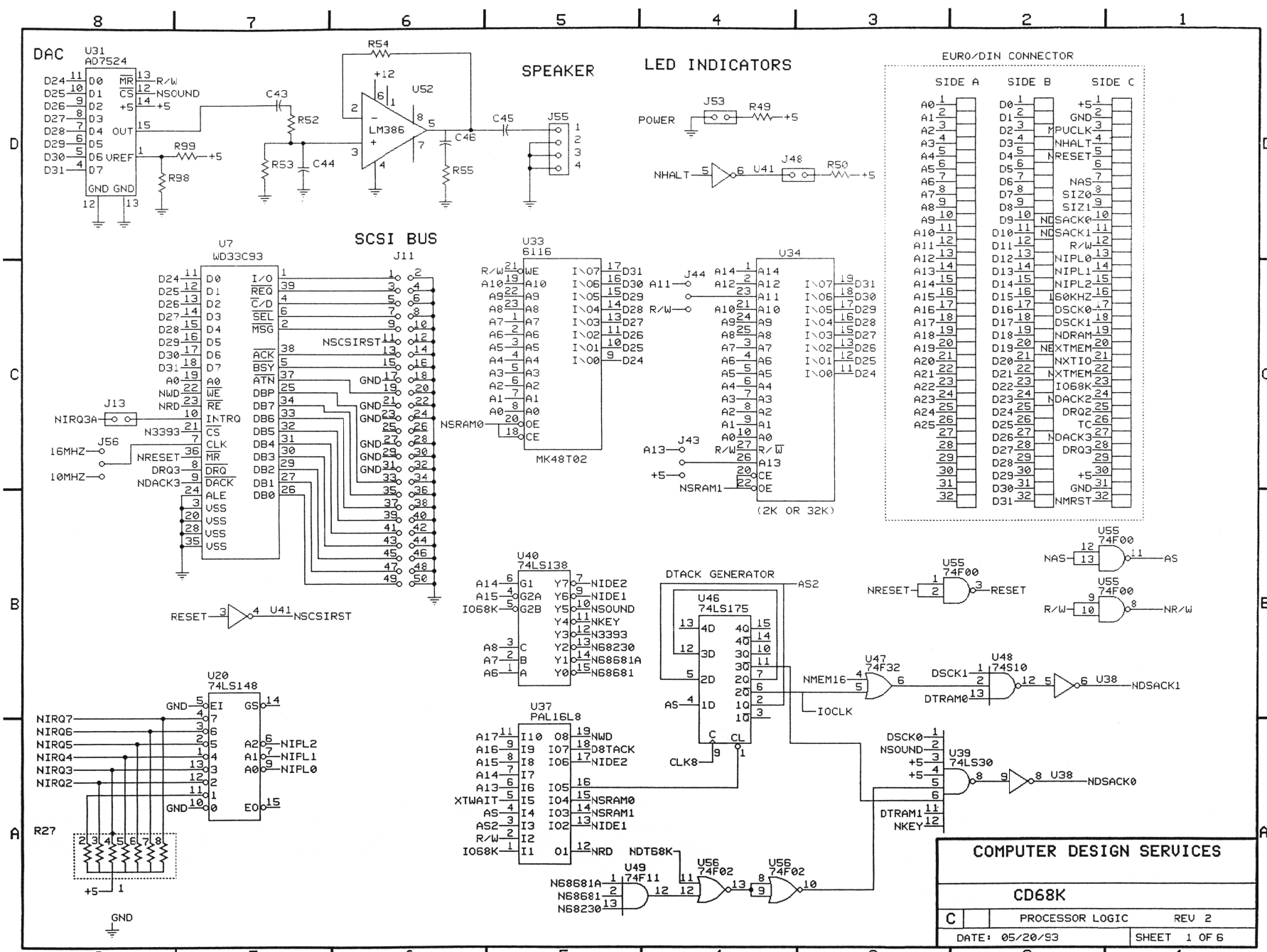
CD68X20 System Board Parts List

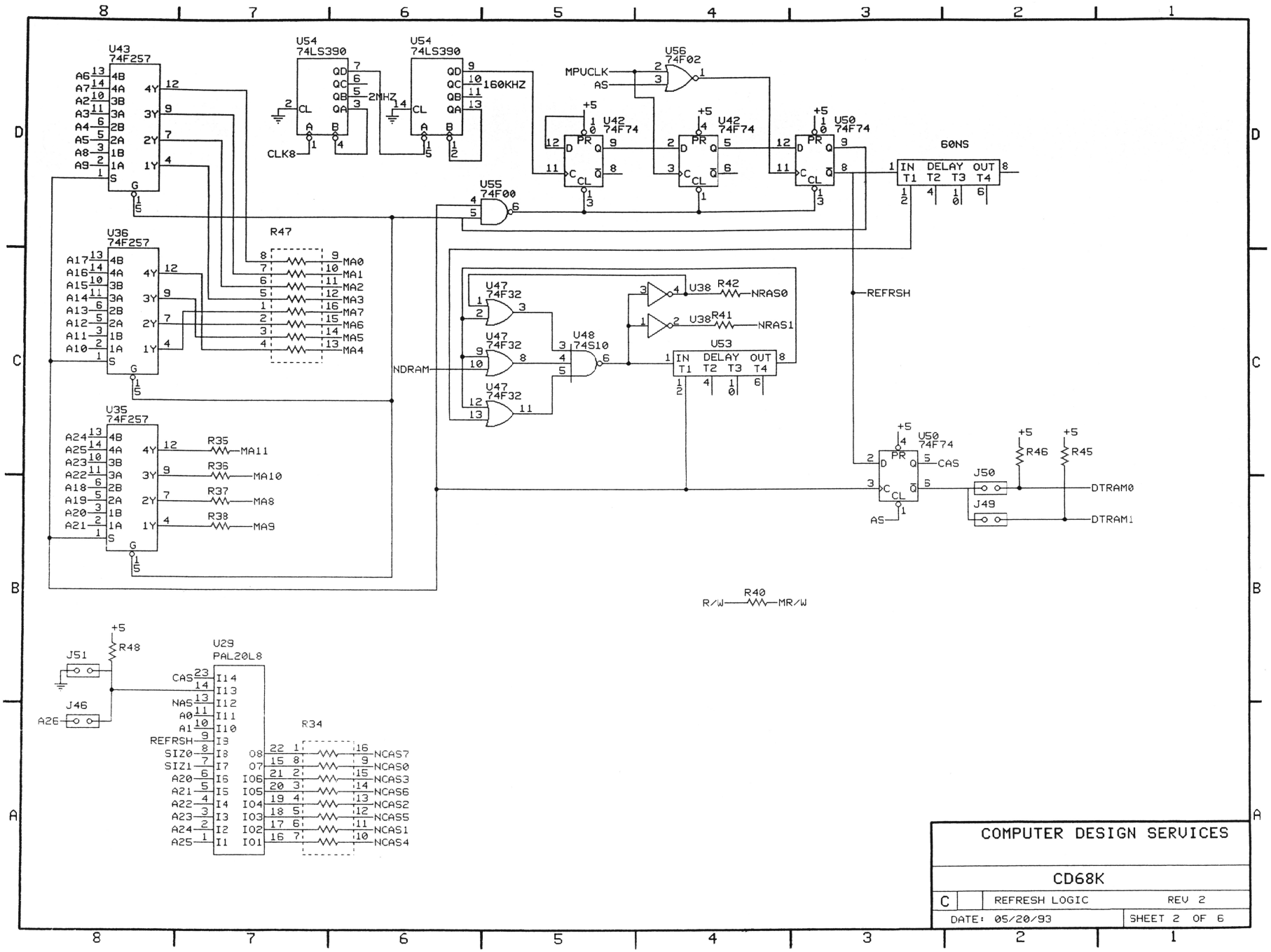
1	J10	5 Pin PC DIN connector
1	J11	25x2 Header Strip
2	J12	Burndy Connector
7	J13,J14,J51,J48,J53,J54	2x1 Header Strip
4	J15,J43,J44,J56	3x1 Header Strip
2	(J20-J21),(J49-J50)	2x2 Header Strip
5	(J22-J24),(J25-J27) (J28-J30),(J31-J33) (J34-J36)	3x2 Header Strip
5	J37-J41	36 Pin AT Connector
2	J42,J47	20x2 Header
1	J45	96 Pin Female DIN Connector
1	J51	4x1 Header Strip
1		8 Pin IC Socket
20		14 Pin IC Socket
10		16 Pin IC Socket
11		20 Pin IC Socket
2		24 Pin IC Scoket (300 mil width)
1		24 Pin IC Socket (600 mil width)
1		28 Pin IC Socket
4		Dual Vertical SIMM Sockets
4	R1,R54,R98,R99	1K Ohm 1/4W Resistor
15	R2,R3,R5,R6,R13,R19 R28,R29,R30,R32,R33, R48,R43,R45,R46	10K Ohm 1/4W Resistor
6	R7-R11,R51	150 Ohm 1/4W Resistor
3	R4, R12, R31	2200 Ohm 1/4W Resistor
2	R49,R50	330 Ohm 1/4W Resistor
10	R15,R16,R17,R18 R21-R26	33 Ohm 1/4W Resistor
6	R36,R35,R37,R38,R41,R42	10 Ohm 1/4W Resistor
1	R34	33 Ohm Dip Resistor Pack
1	R47	10 Ohm Dip Resistor Pack
1	R27	8 Pin 10K Sip Resistor Pack
2	R14,R20	8 Pin Sip 470 Ohm Resistor Pack
1	R52	4700 Ohm 1/4W Resistor
10		Shorting Shunts
1		Board
35		0.1uF Capacitor
3	C3,C4,C5	47pF Capacitor
1	C44	.0047uF Capacitor
1	C45	220uF 16V Capacitor
1		100uF 16V Capacitor
1	U4	Oscillator Socket

Parts List CDS68020

1	U1	27128/27256/27512 EPROM
1	U2	27128/27256/27512 EPROM
1	U3	PAL22V10-15
1	U4	50MHZ OSC
1	U5	74F74
1	U6	MC68020P25
1	U7	MC68882P25
1	U8	74LS164
1	U9	7406
1	U10	74LS175
1	U11	555
1	U12	74F04
4	R1,R2,R13,R14	33 Ohm 1/4W
2	R3,R5	2200 Ohm 1/4W
2	R4,R6	150 Ohm 1/4W
3	R7,R8,R12	10k Ohm 1/4W
1	R9	1M Ohm 1/4W
2	R10,R11	1K Ohm 1/4W
9	C1-C6,C8,C9,C13	0.1uF
3	C7,C10,C11	10uF Tant 16V
2	J1,J3	3x1 Header Strip
3	J2,J4,J6	2x1 Header Strip
1	J5	96 Pin DIN Right Angle Connector
1	U3	24 Pin 300 mil-width IC Socket
1	U11	8 Pin IC Socket
4	U5,U8,U9,U12	14 Pin IC Socket
1	U10	16 Pin IC Socket
2	U1,U2	28 Pin IC Socket
1	U6	114 Pin PGA Socket
1	U7	68 Pin PLCC Socket
3		Shorting Shunts
1		Board


U4
50 MHZ
U5
74F74
U6
68020
U7
68881
PLCC
EURO/DIN CONNECTOR
SIDE A
SIDE B
SIDE C
U10
74LS175
U11
LM555
U12
U9
U8
74LS164
U3
PAL20L10
U1
27512
U2
27512
J1
J2
J3
J4
J6
C1
C2
C3
C4
C5
C6
C10
C11
10uF Tant
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
C7
C8
C9
MPUCLK
160KHZ
NAS
RESET
NHALT
NRESET
NMAP
NDRAM
D8TACK
NXTIO
NXTMEM
NECS
CS68881
NROM0
NROM1
NAVEC
NG68IO
CACHE CONTROL
SHORTED=DISABLED
BOOT EPROM
SHORTED=U1
OPEN=U2
EPROM J1 J3
27128 1 1
27256 1 2
27512 2 2
A26 A27 A28
0 0 1 XTMEM
1 0 1 XTI/O
0 1 1 SRAM/ROM
1 1 1 68K I/O
COMPUTER DESIGN SERVICES
68020 PROCESSOR
PROCESSOR LOGIC
REV 2
DATE: 05/20/93
SHEET 1 OF 1


DAC
U31
AD7524
R54
+12
U52
LM386
C43
R52
C44
R53
C45
C46
R55
J55
R99
R98
SPEAKER
LED INDICATORS
POWER
J53
R49
NHALT
J48
R50
U41
EURO/DIN CONNECTOR
SIDE A
SIDE B
SIDE C
SCSI BUS
U7
WD33C93
J11
J13
NIRQ3A
J56
16MHZ
10MHZ
NRESET
U33
6116
MK48T02
NSRAM0
U34
J44
J43
NSRAM1
(2K OR 32K)
RESET
NSCSIRST
U40
74LS138
U37
PAL16L8
U20
74LS148
R27
DTACK GENERATOR
U46
74LS175
AS2
IOCLK
CLK8
U47
74F32
U48
74S10
U38
NDSACK1
U39
74LS30
NDSACK0
U49
74F11
U56
74F02
U55
74F00
NAS
AS
NR/W
COMPUTER DESIGN SERVICES
CD68K
C
PROCESSOR LOGIC
REV 2
DATE: 05/20/93
SHEET 1 OF 6



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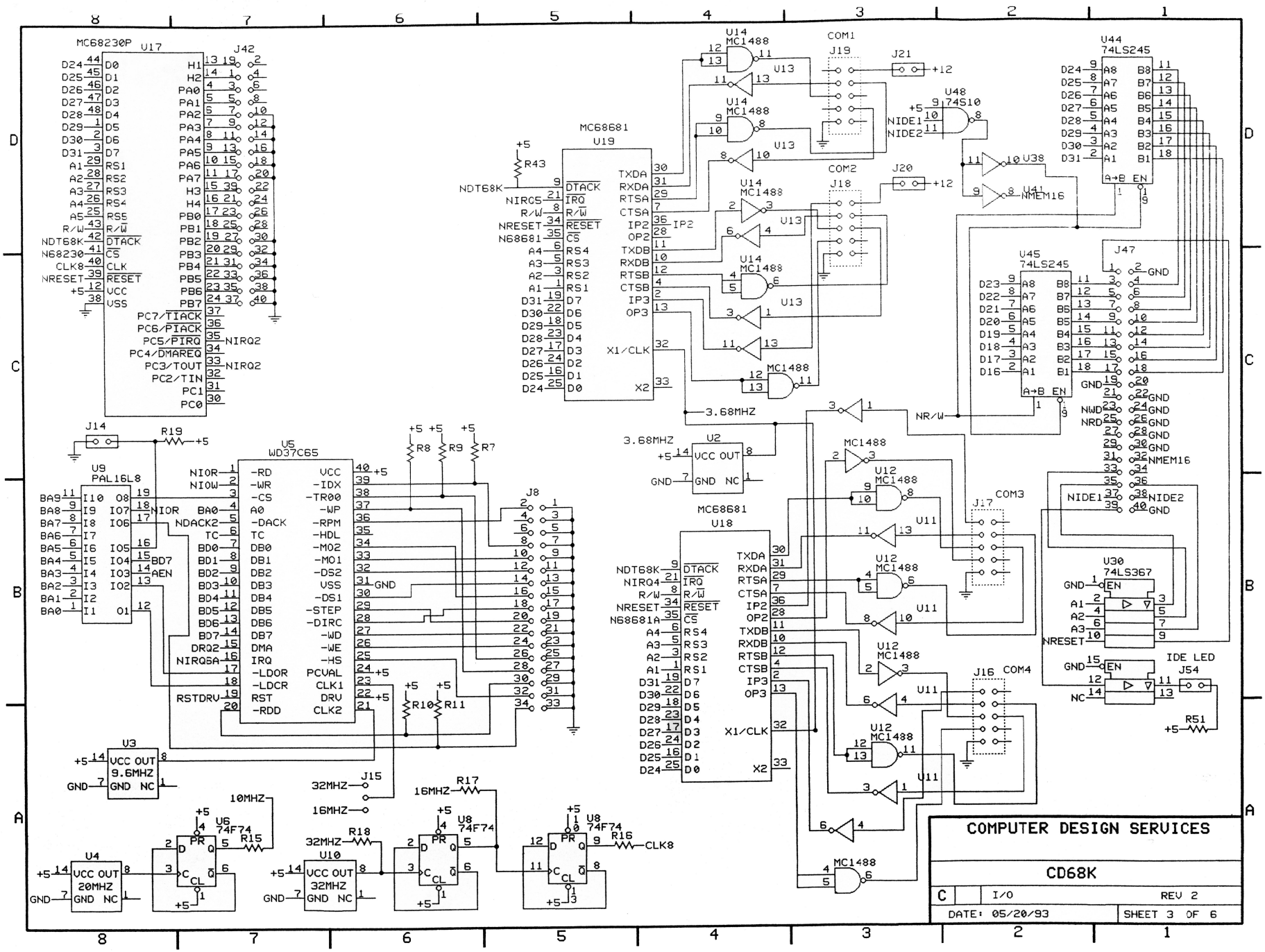
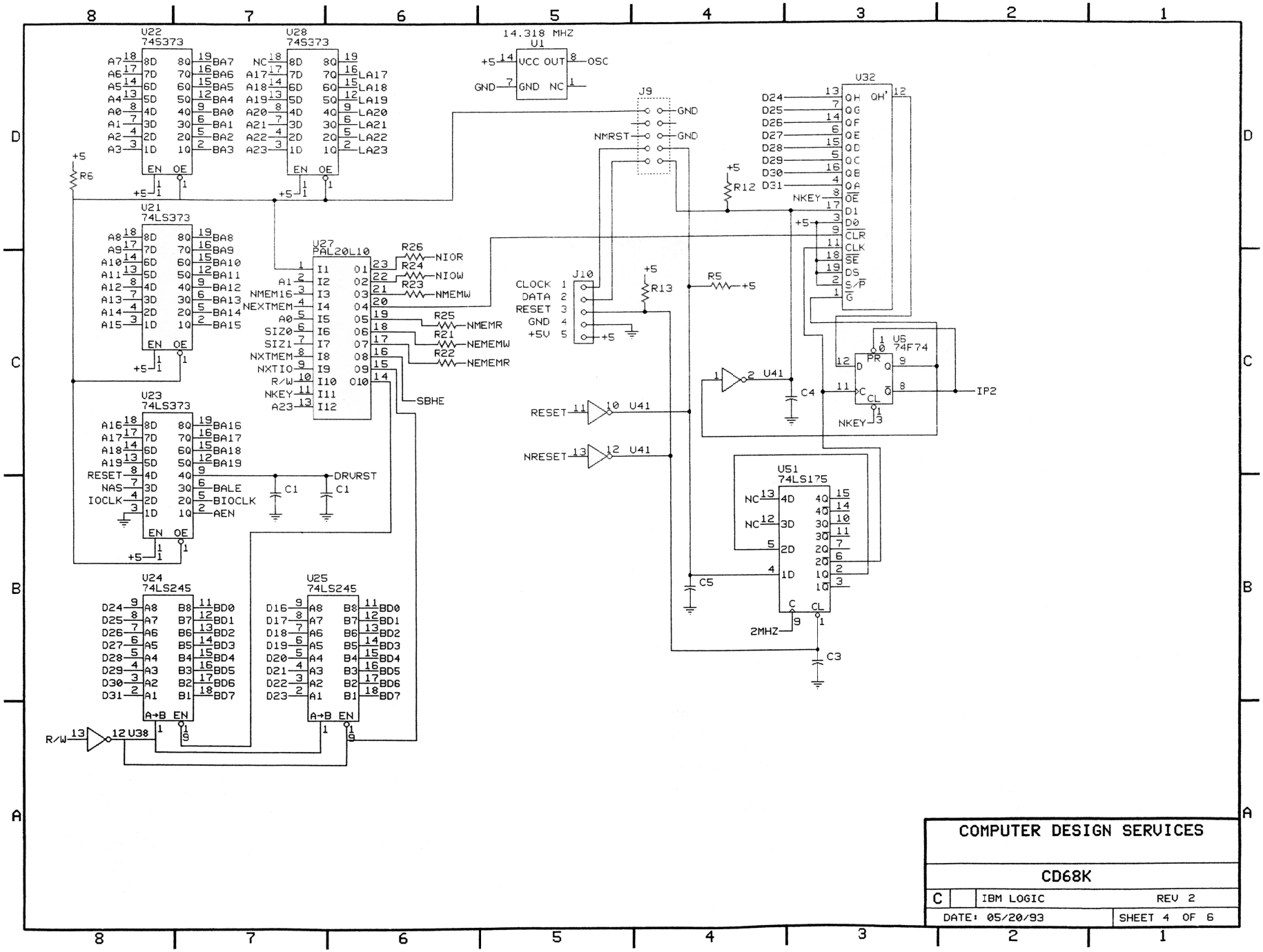
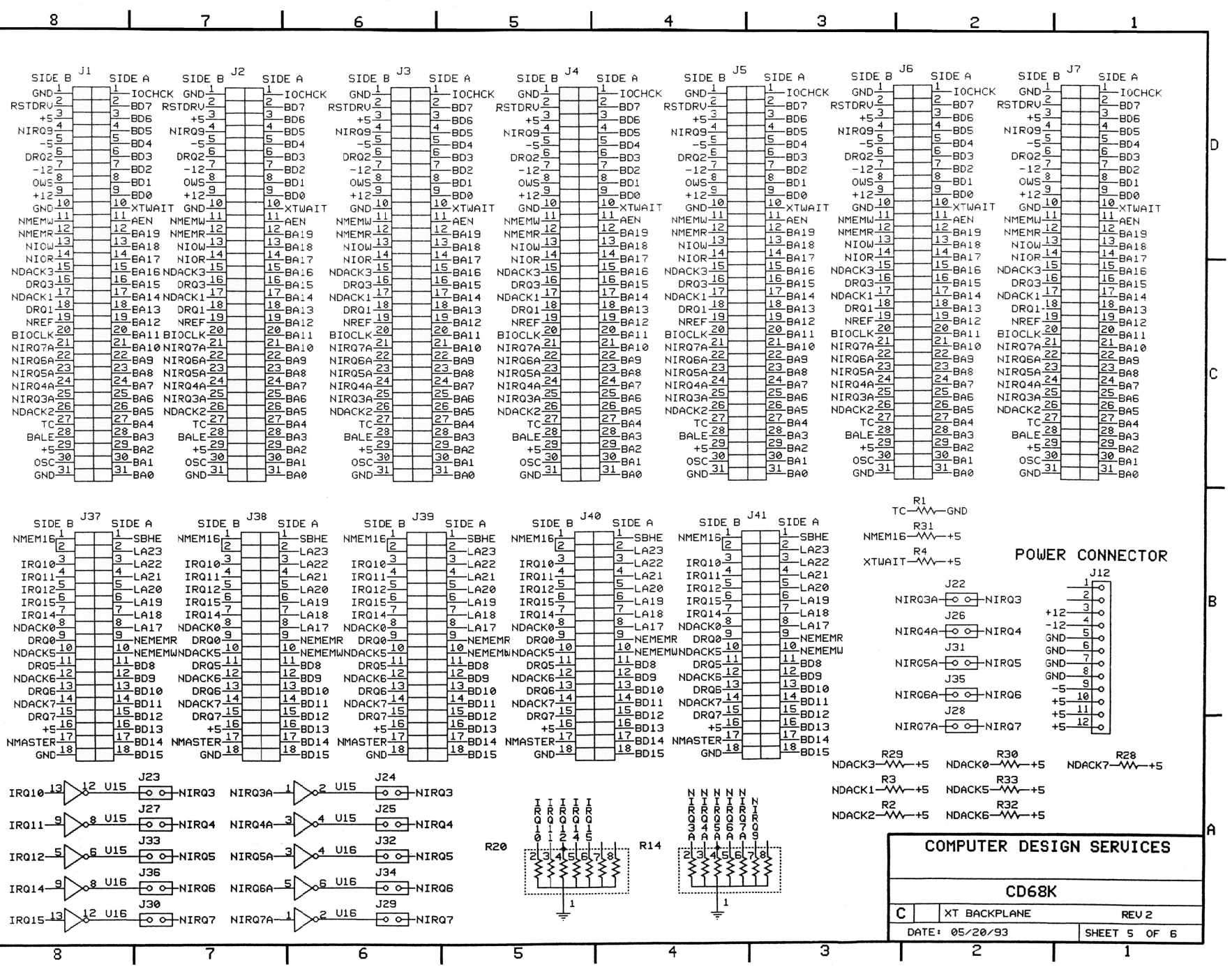
CD68K			
C		REFRESH LOGIC	REV 2
DATE: 05/20/93			SHEET 2 OF 6


COMPUTER DESIGN SERVICES
CD68K
C
I/O
REV 2
DATE: 05/20/93
SHEET 3 OF 6
MC68230P U17
MC68681 U19
MC68681 U18
U14 MC1488
U13
COM1
COM2
COM3
COM4
J19
J18
J17
J16
J21
J20
+12
U48 74S10
NIDE1
NIDE2
U38
U41
NMEM16
U44 74LS245
U45 74LS245
J47
GND
NWD
NRD
R43
NDT68K
NIRQ5
R/W
NRESET
N68681
3.68MHZ
U2
NR/W
U5 WD37C65
U9 PAL16L8
NIOR
NIOW
NDACK2
TC
BD7
AEN
GND
R19
R8
R9
R7
J8
R10
R11
U3
9.6MHZ
J14
J15
32MHZ
16MHZ
R17
R18
R15
R16
U4
20MHZ
U6 74F74
U8 74F74
U10
10MHZ
CLK8
U30 74LS367
IDE LED
J54
R51
NRESET


U22
74S373
U28
74S373
14.318 MHZ
U1
VCC OUT
GND NC
OSC
J9
GND
NMRST
U32
R6
R12
U21
74LS373
U27
PAL20L10
R26
NIOR
R24
NIOW
R23
NMEMW
R25
NMEMR
R21
NEMEMW
R22
NEMEMR
SBHE
J10
CLOCK
DATA
RESET
GND
+5V
R13
R5
U5
74F74
IP2
C4
U41
U23
74LS373
DRVRST
C1
U51
74LS175
C5
C3
2MHZ
U24
74LS245
U25
74LS245
R/W
U38
COMPUTER DESIGN SERVICES
CD68K
C
IBM LOGIC
REV 2
DATE: 05/20/93
SHEET 4 OF 6


J1
J2
J3
J4
J5
J6
J7
SIDE B
SIDE A
GND
RSTDRV
+5
IRQ9
-5
DRQ2
-12
OWS
+12
GND
MEMW
MEMR
IOW
IOR
DACK3
DRQ3
DACK1
DRQ1
REF
BCLK
IRQ7
IRQ6
IRQ5
DACK2
TC
ALE
+5
OSC
GND
IOCHCK
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
XTWAIT
AEN
BA19
BA18
BA17
BA16
BA15
BA14
BA13
BA12
BA11
BA10
BA9
BA8
BA7
BA6
BA5
BA4
BA3
BA2
BA1
BA0
J37
J38
J39
J40
J41
MEMW
MEMR
SBHE
LA23
LA22
LA21
LA20
LA19
LA18
LA17
MEMR
MEMW
IRQ10
IRQ11
IRQ12
IRQ15
IRQ14
DACK0
DRQ0
DACK5
DRQ5
DACK6
DRQ6
DACK7
DRQ7
MASTER
BD8
BD9
BD10
BD11
BD12
BD13
BD14
BD15
R1
TC
GND
R31
MEMW
+5
R4
XTWAIT
+5
POWER CONNECTOR
J12
J22
IRQ3
J26
IRQ4
J31
IRQ5
J35
IRQ6
J28
IRQ7
R29
DACK3
R3
DACK1
R2
DACK2
R30
DACK0
R33
DACK5
R32
DACK6
R28
DACK7
J23
J27
J33
J36
J30
J24
J25
J32
J34
J29
U15
U16
R20
R14
COMPUTER DESIGN SERVICES
CD68K
C
XT BACKPLANE
REV 2
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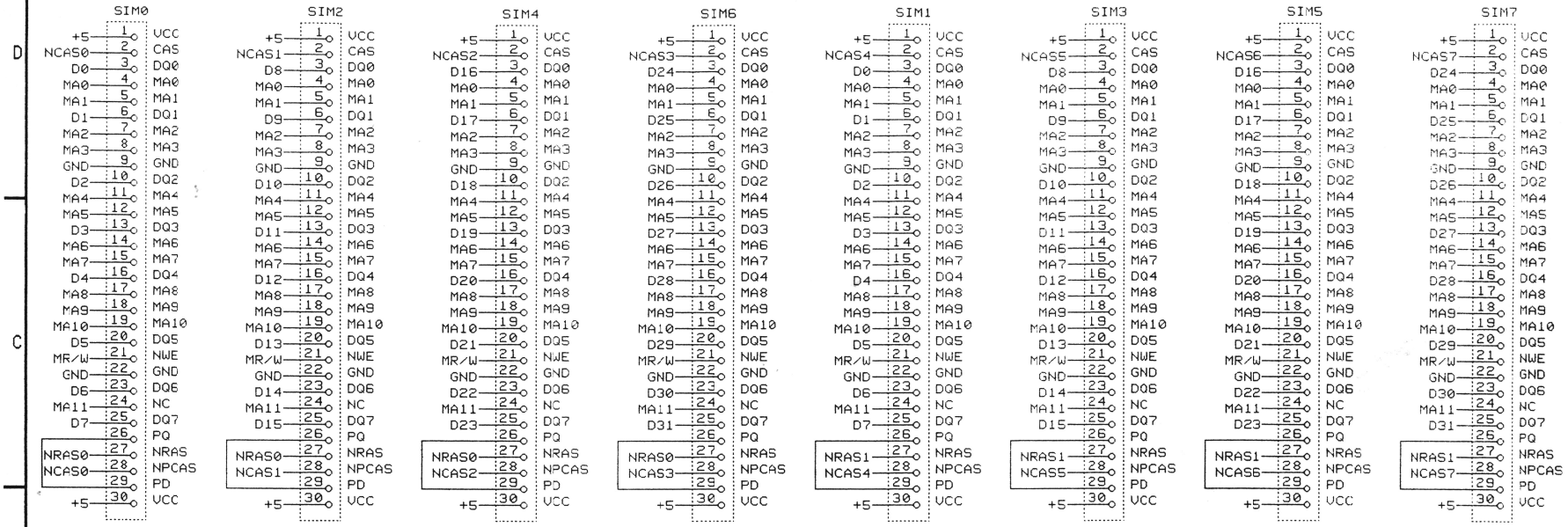
SHEET 5 OF 6



DATA	BANK 0	BANK 1
D0-D7	SIM0	SIM1
D8-D15	SIM2	SIM3
D16-D23	SIM4	SIM5
D24-D31	SIM6	SIM7

COMPUTER DESIGN SERVICES

CD68K

C | | MEMORY | REV 2

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